TF-A Tech Forum
A Class Architecture Automotive Enhance (AE) support

Manish Pandey, Manish Badarkhe
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## Introduction

### Goals
- To use TF-A in Safety critical platforms
- Support AE variants of Arm HW IP, primarily GIC and CPU
- Understanding partner's use cases
- Based on feedback, prioritizing and planning
- Generic implementation as much as possible
- Co-development with partners and possibly validating on their platforms
- Setup regular sync-up with interested partners

### GIC-600AE
- GIC-600 + Fault Management Unit
- FMU accessible to R-Class processor in platform
- TRM available publicly but no support in TF-A yet

### Story So far
- Mailing list discussion started [https://lists.trustedfirmware.org/pipermail/tf-a/2021-January/000946.html](https://lists.trustedfirmware.org/pipermail/tf-a/2021-January/000946.html)
- Platform not available
- Identified tasks which can be carried out without availability of platform
- Feature parity between GIC-600 and GIC-600AE
- Disable GICR frames for fused-off cores, patches under review [https://review.trustedfirmware.org/c/TF-A/trusted-firmware-a/+/8150/6](https://review.trustedfirmware.org/c/TF-A/trusted-firmware-a/+/8150/6)
Identified tasks

• Feature Parity between GIC-600 and GIC-600AE (Finished)

• GIC FMU RAS Extensions
  • FMU detection by detecting GIC-600AE part number (Arm)
  • FMU initialization
  • Error injection

• Dual Core Lock-Step (DCLS) mode
  • Number of PEs statically defined, need to make it dynamic (Arm)
  • Any changes in GIC to support Lock mode?

• Enhancements of existing GIC Driver
  • Read trace and PMU records (Arm)
  • Keep RAS error records alive across a reset (Arm)
  • Disable GICR frames of fused-off cores (Patches under review)
  • Support for message signalled interrupts
  • Saving/Restoring additional GIC registers during PM events (Arm)

  *(Arm) : Arm will start working on it*
Thank You
Danke
Gracias
谢谢
ありがとう
Asante
Merci
감사합니다
धन्यवाद
Kiitos
شكرًا
ধন্যবাদ
תודה