GIC600AE\textsuperscript{1} Fault Management Unit (FMU)

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\textsuperscript{1}https://developer.arm.com/documentation/101206/0000
Overview

Differences with GIC600

New Registers
  Global
  Error Records

TF-A Impact
  RAS & SDEI
  Testing
  Options & Challenges
Differences with GIC600

- GIC features compatible with GIC600
- Unit to collect errors (FMU)
- Duplicated logic in GIC structures
- ECC in RAMs
- Store correctable and uncorrectable errors
- Dedicated bus for error reporting
# FMU Registers

<table>
<thead>
<tr>
<th>Offset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000 + 64n</td>
<td>4×u64</td>
<td>Error Records, Details on next slide</td>
</tr>
<tr>
<td>0xE00</td>
<td>u64</td>
<td>Error Present, 1 bit for each record</td>
</tr>
<tr>
<td>0xEA0</td>
<td>u32</td>
<td>Lock, writing key enables a write</td>
</tr>
<tr>
<td>0xEB4</td>
<td>u32</td>
<td>Safety Mechanism Enable, on at boot</td>
</tr>
<tr>
<td>0xEC0</td>
<td>u32</td>
<td>Error Injection</td>
</tr>
<tr>
<td>0xF00</td>
<td>u32</td>
<td>FMU Idle Status</td>
</tr>
<tr>
<td>0xFC8</td>
<td>u32</td>
<td>Number of Error Records</td>
</tr>
<tr>
<td>Offset</td>
<td>Width</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>------------------------------------------------------------</td>
</tr>
<tr>
<td>0x00</td>
<td>u64</td>
<td>Present: Fault &amp; Recovery Interrupts &amp; Logging</td>
</tr>
<tr>
<td>0x08</td>
<td>u64</td>
<td>Control: Fault &amp; Recovery Interrupts &amp; Logging</td>
</tr>
<tr>
<td>0x10</td>
<td>u64</td>
<td>Status: Valid, Code, Overflow, Correctable etc.</td>
</tr>
<tr>
<td>0x18</td>
<td>u64</td>
<td>Unspecified: Probably Read as Zero</td>
</tr>
</tbody>
</table>
RAS & SDEI Integration

- Define a dispatcher for the GIC600AE FMU
- Encode Error records as SDEI_EXPLICIT_EVENT
- Dispatch Correctable errors through SDEI
- Panic on Uncorrectable errors
For each error type

- Register with SDEI
- Cause an interrupt w/ Error Injection Reg
- Handle Error by setting flag
- Assert flag was set
Implementation Options & Challenges

- Correctable Errors
  - Treat as Uncorrectable?
  - Dispatch every?
  - Dispatch on overflow?

- Report Uncorrectable Errors to BMC/SCP?

- Disable Safety Mechanism before enable interrupts?